9. (Once Amended) A method according to Claim 7, wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from [of] about 1:1 to about 2:1.

14. (Once Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding electrically active region below the termination of said each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers; and

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selectively removing said conformal second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

31. (Once Amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a conformal second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers; and

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planarizing said conformal second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

7 32. (Once Amended) A method according to Claim 31, wherein each said liner is a thermally grown oxide of said semiconductor substrate, and wherein said conformal second layer is composed [on] of an electrically [conductive] insulative material.

7 33. (Once Amended) A method according to Claim 31, wherein each said liner is composed of silicon nitride, and wherein said conformal second layer is composed [on] of an electrically [conductive] insulative material.

35. (Twice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer[;], wherein said spacer and said isolation trench are formed with a single etch recipe;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

38. (Twice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer[;], wherein said spacer and said isolation trench are formed with a single etch recipe; (how can?) P.11

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

41. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface;

forming first and second isolation trenches each:

extending into and being defined by the semiconductor substrate;

having an opening thereto at the top surface of the semiconductor substrate; and

extending below and being centered between a pair of spacers situated above the top surface of the semiconductor substrate[;], wherein said spacers and said isolation trenches are formed with a single etch recipe;

and wherein:

an electrically insulative material extends continuously between and within the first and second isolation trenches; and

a planar surface begins at the first isolation trench and extends continuously to the second isolation trench; and

wherein the microelectronic structure is defined at least in part by the pair of spacers, the electrically insulative material, and the first and second isolation trenches.

42. (Twice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said

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first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

forming a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Twice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench;

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a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, conformally filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

planarizing the conformal second layer and said first and second spacers of said respective first and second isolation structures to form [forming] a planar upper surface [formed] from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches.